REMARKS/ARGUMENTS

Prior to this amendment, claims 1-34 were pending. In this amendment, claims 1, 10, 18, 20, 29, 31 and 33 are been amended. Claim 30 is canceled. New claims 35-36 are added. No new matter has been added. Thus, after entry of this amendment, claims 1-29 and 31-36 will be pending. Reconsideration of the rejected claims is respectfully requested.

Rejection under 35 U.S.C. § 101

Claims 29-34 are rejected under 35 U.S.C. § 101 for being directed to non-statutory subject matter.

Claim 29 recites a tangible result of obtaining the at least part of a total sum of the binary numbers according to the claimed method, as well as outputting the at least part of the total sum of the binary numbers from the adder. Accordingly, Applicants respectfully request withdrawal of these rejections.

Rejection under 35 U.S.C. 102(b), Baeckler

Claims 1-34 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Baeckler (herein "Baeckler"). A Petition to Expunge enclosed herewith has been submitted to expunge Baeckler. Baeckler is a confidential document that has not been made publicly accessible and thus is not a printed publication under 35 U.S.C. § 102. Accordingly, Baeckler is not prior art. Accordingly, Applicants respectfully request withdrawal of these rejections.

Rejection under 35 U.S.C. 102(b), Rothman

Claims 1, 3, 8, 9, 29 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Rothman et al, (5,898,602).

Claims 1-9

Claim 1 is allowable as Rothman does not teach or suggest each and every element of claim 1. For example, claim 1 recites:

> *a first look-up table (LUT) in a first logic element (LE), wherein the first LUT produces a carry from a first set of corresponding bits of at least three binary numbers; and*
>
> *a second LUT in a second LE, wherein the second LUT produces a sum from a second set of corresponding bits of the binary numbers; and*

an adder in the second LE, wherein the adder is coupled with the first LUT and the second LUT, and wherein the adder adds the carry and the sum.

In Rothman, an arithmetic logic cell ALU sums the value of two binary numbers A and B. *See Rothman*, FIG. 4 and col. 2 lines 12-23. A carry cell 10 has inputs of bits of the two binary numbers and carry signal from another ALU. *Id.* Adder blocks 15 add the two input bits of the two binary numbers and the carry signal is added by another XOR gate. *Id.*, FIG. 4 and col. 2 lines 60-63.

As described, the ALU configuration of FIG. 4 only computes a carry and sum of two binary numbers. In contrast, claim 1 recites producing a carry and sum of at least three binary numbers. Moreover, the configuration of FIG. 4 is not suitable for adding three binary numbers.

Additionally, FIG. 5 shows carry cell 10 replaced by a LUT 30, and adder block 15 replaced by LUT 50. Rothman does not mention another adder circuit. Thus, Rothman does not teach an adder that is coupled with the first LUT and the second LUT, as recited in claim 1.

For at least these reasons, claim 1 is allowable over Rothman. As claim 1 is allowable, dependent claims 2-9 are also allowable for at least the same rationale.

Claims 29, 31-36

Applicants submit that claim 29 should be allowable for at least the same rationale as discussed with respect to claim 1. As claim 29 is allowable, dependent claims 31-36 are allowable for at least the same rationale.

Rejection under 35 U.S.C. 102(b), New

Claims 1, 3, 8, 9, 29, 30 are rejected under 35 U.S.C. 102(b) as being anticipated by New (6,288,570).

Claims 1-9

Similarly, as for Rothman, New is directed to adding two binary numbers. *See New*, abstract. In contrast, claim 1 recites producing a carry and sum of at least three binary numbers.

Additionally, New does not teach or suggest a first LUT producing a carry. In New, the function generator 903 sums two bits of A and B, and does not produce a carry. *See*

New, FIG. 8b and col. 6 lines 49-53. The carry is either A_i or the old carry, and not the sum P_i produced by generator 903. Function generator 904 adds the carry C_i to the sum of the bits of A and B. *Id.* Thus, function generator 903 produces a sum and not a carry.

Moreover, the function generator 904 is in a different CLB than function generator 903. *Id.*, col. 14 lines 45-48. In contrast, claim 1 recites that the adder is in the second LE, in which the second LUT, which produces the sum, also resides.

For at least these reasons, claim 1 is allowable over New. As claim 1 is allowable, dependent claims 2-9 are also allowable for at least the same rationale.

Claims 29, 31-36

Applicants submit that claim 29 should be allowable for at least the same rationale as discussed with respect to claim 1. As claim 29 is allowable, dependent claims 31-36 are allowable for at least the same rationale.

Rejection under 35 U.S.C. 102(b), Cohen

Claims 10, 11, 16-19, 23 and 24, are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen et al. (5,511,017), which was incorrectly cited as Hara et al. (5,764,557) in the Office Action.

Claims 10-17

Claim 10 is allowable as Cohen does not teach or suggest each and every element of claim 10. For example, claim 10 recites "*wherein the multiplexer selects the signal determined in the previous LE when the LE is set to operate in an addition of three binary numbers mode.*"

In FIG. 6, multiplexer 33 selects between a component X on bus 12 that has been extended with zeros with extender 17 and a correction term 37 that is added to the incorrect sum recirculated from register 25 in a subsequent calculation step. *See Cohen*, col. 6 lines 23-35 and lines 59-62. Thus, multiplexer 33 selects correction term 37 when a subsequent calculation step is being performed by adder 35, and not when multiplexer 33 is set to an addition of three binary numbers mode. Accordingly, Cohen does not teach or suggest the multiplexer selecting the

signal determined in the previous LE when the LE is set to operate in an addition of three binary numbers mode.

For at least these reasons, claim 10 is allowable over Cohen. As claim 10 is allowable, dependent claims 11-17 are also allowable for at least the same rationale.

Claims 18-24

Claim 18 is allowable as Cohen does not teach or suggest each and every element of claim 18. For example, claim 18 recites

> *a first logic element (LE) including a first logic circuit, wherein the first logic circuit determines a carry in a carry save adder process, wherein the first LE includes a first look-up table (LUT) that produces a carry from a first set of corresponding bits of at least three binary numbers and*
> *a second LE, wherein the second LE receives the carry.*

At page 4, the Office Action asserts that the first LE includes CSA cell 32-0 that determines carry C0 and that the second LE includes the CSA cell 32-1. However, the carry signal C0 from CSA cell 32-0 is received by full adder cell 34-1 and not CSA cell 32-1. *See* Cohen, FIG.4 and col. 5 lines 31-40. Thus, CSA cell 32-1 does not teach or suggest a second LE that receives a carry determined by a first LE in a carry save adder process, as recited in claim 18. Furthermore, Cohen does not teach or suggest a look-up table that produces a carry. For at least these reasons, claim 18 is allowable over Cohen. As claim 18 is allowable, dependent claims 19-24 are also allowable for at least the same rationale.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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